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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,125	ROONEY ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL OFFICE ACTION

1. This office action is in response to Applicants' Amendment of *13 May 2004*.

1.1 **Claims 1, 4-8, 10,** and **13-18** are amended, **Claims 2, 11** are cancelled. **Claims 1,3-10 and 12-19** remain pending.

1.2 The **prior art** rejections of record are maintained in response to Applicants' amendment.

1.2.1 The objections of record are withdrawn in response to Applicants' amendment.

Response to Arguments

1.3 Applicants' arguments of *13 May 2004* have been fully considered, are persuasive only to the extent that the step of subset compression is not specifically described in detail by **prior art** of record. Said step is clarified and is further supported by newly found references from, e.g., IBM Technical Disclosure Bulletin, as follows.

REMARKS

1.4 In response to **Claims 1, 10,** on pages 9-14, Applicants' arguments/amendment, re: testing of memory address portion as opposed to testing of entire memory address space, are not persuasive such is not in the claims at bar, which recite "wherein the address spaces comprises x addresses and y addresses of the device," implying that the entire memory is tested.'

Assuming the contrary, the compressed subset string so obtained for a partial area of the memory device would not provide full fault coverage.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2.0 Claims 5-6, 14-15, stand rejected under 35 USC § 112 SECOND PARAGRAPH for failing to particularly point out and distinctly define the subject matter which the applicant regards as his invention.

2.1 As per Claims 1, 10, and intervening claims: it is not clear to the Examiner where the bit error rate is estimated

2.1 As per Claims 5-6, 14-15, and intervening claims:

There is a lack of antecedent basis in resp. lines 1 for "executing the test" and determining the test."

Claim Objections

2.2 The claims are objected to for including in passim "address spaces" instead of "address space." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3.1 Claim(s) 1, 3-9 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. U.S. Patent No. 5,961,653 (hereinafter Kalter) in view of Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra) in further view of Hosokawa et al. U.S. Patent No. 6651206.

As per claim 1,

Kalter substantially teaches of using test patterns (that contain address sequencing (i.e. which addresses to test in order) to test portions of the address space, see column 1 lines 45-50. Kalter further of repeating the test patterns a plurality of times, see column 1 lines 47-50 where Kalter teaches of the test pattern continuously changing as the process matures. Since the process changes as it matures, the examiner is interpreting that the process is repeated plural times in order to mature and therefore go through changes.

Kalter does not explicitly teach of including at least an x and a y address, or of testing every combination by holding each address at a first potential and a second potential, or of determining and combining pass/fail information into a fail string. Nonetheless, Kalter does teach of using test patterns to test memories using data patterns, address sequencing and timing sequences, see column 1 lines 45-50.

Schanstra, in an analogous art, teaches of storing memory in a two-dimensional (i.e. x and y dimensions) array of memory cells, see section 2, column 2 on page 872. Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads. Schanstra further teaches of using the pass/fail results of the read operations (tests), see section 2.1 column 1 on page 873. Further, Schanstra teaches that the bitmap is dependant upon the memory test algorithm used. It is clear that if only a certain section memory is to be tested (i.e. the test pattern address sequence) then the resulting bitmap will contain pass/fail information of the cells tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory testing of Kalter to include the teachings of Schanstra so as to enhance the memory testing capability of Kalter. This modification would have been obvious because of one ordinary skill in the art would have been motivated by the fact that the cited teachings of Schanstra are described as "the principles of memory testing and bit mapping," see column 1, last paragraph of section 1 on page 872 and as a result would have been both an easy and obvious step to include and implement.

While **Schanstra and Kalter** substantially disclose the procedure for the claimed invention, they fail to specifically describe in detail that string compression is effected.

However, **Hosokawa** describes in detail fault string compression via fault string combining in Figs. 49-59 to reduce testing overhead.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Schanstra and Kalter** by including therein fault string compression as taught by **Hosokawa**, because such modification would provide the procedure disclosed in **Schanstra and Kalter** with a technique whereby test vector memory requierements are optimized. {See **Hosokawa**, Id., Figs. 49-59.}

As per claim 3,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include a single address. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 4,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to hold the test pattern at a first potential and yield a pass/fail as well as to hold the test pattern at a second potential to yield a pass/fail. One of ordinary skill in the art would want to hold the test pattern at a first potential (i.e. 0) or a second potential (i.e. 1) so as to be able to test for, for example, stuck at high(1)/low(0) faults. Further, since Schanstra teaches of performing multiple reads (tests) per memory cell to obtain pass/fail information (section 2.1 column 1 on page 873), holding the cell at a certain potential long enough so as to obtain a pass/fail result would have been obvious as well. Since the purpose is to determine if a cell has passed or failed a memory test, then it would have been obvious to hold the cell at a value until a determination had been made.

As per claim 5,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include multiple addresses. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 6,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to determine the x and y addresses according to a targeted fail type. One of ordinary skill in the art would have chosen a fail type for testing and then chosen addresses appropriately. Further since only portions/sections/parts of the memory are being tested, then it would have been obvious to one of ordinary skill to select addresses of memory cells that fall within the current section to be part of the test pattern. Clearly, if addresses of cells not within the current section are chosen, then those cells would not be tested. Still further, the since the fail type is known, one of ordinary skill would know the characteristics of the fail type and clearly would have known which addresses to test to be able to detect the selected fault/fail type.

As per claim 7,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it.

As per claim 8,

Schanstra further teaches that a pass/fail cell is marked as a result of the cell passing or failing a test/read operation, see column 1 section 2.1 on page 873. While Schanstra does teach that a cell has failed if at least one test results in a fail, one of ordinary skill could easily lower the conditions for pass/fail so as to allow a pass result if at least one test results in pass or even if a certain percentage results in a pass.

As per claim 9,

Schanstra further teaches about the ability of BIST to be able to distinguish between fault types and locate the fault types, see column 2 section 3 on page 873. Since the pareto graph is essentially showing that faults types are not evenly distributed (i.e. only a few faults are responsible for the majority of the memory fails/defects) then it would have been an obvious step to one of ordinary skill in the art to take the fault distinguishing results and record them in the pareto chart/graph so as to be able to determine which faults cause the majority of the failures (i.e. the SC fail type in applicant's figure 1). One would be motivated to be able to determine which faults cause a majority of the failures so as to be able to take actions to prevent/remove those faults thereby causing less failures (and a getting higher yield).

3.1.a Claim(s) 1 and 10 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. U.S. Patent No. 5,961,653 (hereinafter Kalter) in view of Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra) in further view of NN9111377: (Reconfigurable Signature Generator. IBM Tech. Disclosure Bulletin, VOL. # 34 ISSUE # 6, Pgs. 377 - 380, November 1, 1991, hereinafter IBM Tech 7).

As per claims 1 and 10,

Kalter substantially teaches of using test patterns (that contain address sequencing (i.e. which addresses to test in order) to test portions of the address space, see column 1 lines 45-50. Kalter further of repeating the test patterns a plurality of times, see column 1 lines 47-50 where Kalter teaches of the test pattern continuously changing as the process matures. Since the

process changes as it matures, the examiner is interpreting that the process is repeated plural times in order to mature and therefore go through changes.

Kalter does not explicitly teach of including at least an x and a y address, or of testing every combination by holding each address at a first potential and a second potential, or of determining and combining pass/fail information into a fail string. Nonetheless, Kalter does teach of using test patterns to test memories using data patterns, address sequencing and timing sequences, see column 1 lines 45-50.

Schanstra, in an analogous art, teaches of storing memory in a two-dimensional (i.e. x and y dimensions) array of memory cells, see section 2, column 2 on page 872. Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads. Schanstra further teaches of using the pass/fail results of the read operations (tests), see section 2.1 column 1 on page 873. Further, Schanstra teaches that the bitmap is dependant upon the memory test algorithm used. It is clear that if only a certain section memory is to be tested (i.e. the test pattern address sequence) then the resulting bitmap will contain pass/fail information of the cells tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory testing of Kalter to include the teachings of Schanstra so as to enhance the memory testing capability of Kalter. This modification would have been obvious because of one ordinary skill in the art would have been motivated by the fact that the cited teachings of Schanstra are described as "the principles of memory testing and bit mapping," see column 1, last paragraph of section 1 on page 872 and as a result would have been both an easy and obvious step to include and implement.

While **Schanstra and Kalter** substantially disclose the procedure for the claimed invention, they fail to specifically describe in detail that string compression is effected.

However, **IBM Tech 7** describes in detail fault string compression via fault string combining (page 2 1st two sentences) to reduce testing overhead wherein **is** disclosed test sequence generation for an integrated circuit, comprising: a buffer length set step of setting a buffer length or means to set length of test vectors or sequence on page 1 last sentence wherein prior to testing procedure, generator polynomial of selectable length 'm' based on fault coverage requirement (page 2 1st two sentences) is stored for a buffer for storing a test sequence; and is subsequently compressed by an LFSR into an n-bit signature) or a test sequence compaction (or test vectors compaction means) step of generating a test sequence for said integrated circuit, in performing sequentially compaction storage of test sequences for respective faults in buffers having said buffer length set in said buffer length set step; loop or feedback examination means (page 2 1st two sentences, wherein means for loop or feedback path generation is provided by selectively setting the value of Ci to either zero or one); means to input said resultant n-bit signature for testing purposes to yield error polynomial E1(x)(2d page circa line 22).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Schanstra and Kalter** by including therein fault string compression as taught by **IBM Tech 7**, because such modification would provide the procedure disclosed in **Schanstra and Kalter** with a technique whereby test vector memory requierements are optimized. {See **IBM Tech 7**, Id., e.g., page 2 1st two sentences.}

3.2 Claim(s) 10, 12-17 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. U.S. Patent No. 5,961,653 (hereinafter Kalter) in view of Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra) in further view of Hosokawa et al. U.S. Patent No. 6651206.

As per claim 10,

Kalter substantially teaches of using test patterns (that contain address sequencing (i.e. which addresses to test in order) to test portions of the address space, see column 1 lines 45-50. Kalter further of repeating the test patterns a plurality of times, see column 1 lines 47-50 where Kalter teaches of the test pattern continuously changing as the process matures. Since the process changes as it matures, the examiner is interpreting that the process is repeated plural times in order to mature and therefore go through changes.

Kalter does not explicitly teach of including at least an x and a y address, or of testing every combination by holding each address at a first potential and a second potential, or of determining and combining pass/fail information into a fail string. Nonetheless, Kalter does teach of using test patterns to test memories using data patterns, address sequencing and timing sequences, see column 1 lines 45-50.

Schanstra, in an analogous art, teaches of storing memory in a two-dimensional (i.e. x and y dimensions) array of memory cells, see section 2, column 2 on page 872. Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads. Schanstra further teaches of using the pass/fail results of the read operations (tests), see section 2.1 column 1 on page 873. Further, Schanstra teaches that the bitmap is dependant upon the memory test algorithm used. It is clear that if only a certain section memory is to be tested (i.e. the test pattern address sequence) then the resulting bitmap will contain pass/fail information of the cells tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory testing of Kalter to include the teachings of Schanstra so as to

enhance the memory testing capability of Kalter. This modification would have been obvious because of one ordinary skill in the art would have been motivated by the fact that the cited teachings of Schanstra are described as "the principles of memory testing and bit mapping," see column 1, last paragraph of section 1 on page 872 and as a result would have been both an easy and obvious step to include and implement.

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it. Further, Schanstra teaches of labeling a cell as a fail if any one of the multiple read/test operation results in a fail, see column 1 section 2.1 page 873. Therefore, the examiner sees the combination of the test results as an AND operation where a pass could be regarded as '1' and a fail as a '0'. By combining using an AND operation, it ensures that either all of the tests are passes or else a fail is generated i.e. 1 AND 1 = 1/pass whereas 1 AND 0 = 0/fail.

Further, it would have been an obvious step to one of ordinary skill in the art to implement a method into programmed instructions that are executable by a storage device. Once the method is known/discovered, one of ordinary skill would easily be able to implement it in hardware using a plurality of devices as well as a set of programmable instructions readable by a program storage device/machine.

While **Schanstra and Kalter** substantially disclose the procedure for the claimed invention, they fail to specifically describe in detail that string compression is effected.

However, **Hosokawa** describes in detail fault string compression via fault string combining in Figs. 49-59 to reduce testing overhead.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Schanstra and Kalter** by including therein fault string compression as taught by **Hosokawa**, because such modification would provide the procedure disclosed in **Schanstra and Kalter** with a technique whereby test vector memory requierements are optimized. {See **Hosokawa**, Id., Figs. 49-59.}

As per claim 12,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include a single address. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 13,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to hold the test pattern at a first potential and yield a pass/fail as well as to hold the test pattern at a second potential to yield a pass/fail. One of ordinary skill in the art would want to hold the test pattern at a first potential (i.e. 0) or a second potential (i.e. 1) so as to be able to test for, for example, stuck at high(1)/low(0) faults. Further, since Schanstra teaches of performing multiple reads (tests) per memory cell to obtain pass/fail information (section 2.1 column 1 on page 873), holding the cell at a certain potential long enough so as to obtain a pass/fail result would have been obvious as well. Since the purpose is to determine if a cell has passed or failed a memory test, then it would have been obvious to hold the cell at a value until a determination had been made.

As per claim 14,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include multiple addresses. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 15,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to determine the x and y addresses according to a targeted fail type. One of ordinary skill in the art would have chosen a fail type for testing and then chosen addresses appropriately. Further since only portions/sections/parts of the memory are being tested, then it would have been obvious to one of ordinary skill to select addresses of memory cells that fall within the current section to be part of the test pattern. Clearly, if addresses of cells not within the current section are chosen, then those cells would not be tested. Still further, the since the fail type is known, one of ordinary skill would know the characteristics of the fail type and clearly would have known which addresses to test to be able to detect the selected fault/fail type.

As per claim 16,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it.

As per claim 17,

Schanstra further teaches that a pass/fail cell is marked as a result of the cell passing or failing a test/read operation, see column 1 section 2.1 on page 873. While Schanstra does teach that a cell has failed if at least one test results in a fail, one of ordinary skill could easily lower the conditions for pass/fail so as to allow a pass result if at least one test results in pass or even if a certain percentage results in a pass.

3.3 Claim(s) 18-19 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra).

As per claim 18,

Schanstra substantially teaches of marking cells as passing or failing during a bitmapping process, see column 1 section 2.1 on page 873. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it. Further, Schanstra teaches of labeling a cell as a fail if any one of the multiple read/test operation results in a fail, see column 1 section 2.1 page 873. Therefore, the examiner sees the combination of the test results as an AND operation where a pass could be regarded as '1' and a fail as a '0'. By combining using an AND operation, it ensures that either all of the tests are passes or else a fail is generated i.e. 1 AND 1 = 1/pass whereas 1 AND 0 = 0/fail.

While Schanstra does not explicitly teach of having the pass/fail results correspond to X and Y address pins, Schanstra does teaches of the memory being stored as a two-dimensional array of memory cells, see column 2 section 2 page 872. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the addresses of the pass/fail results (cells) correspond to X and Y address pins. One of ordinary skill in the art would know that memory (i.e. those in array form) are addressable through pins. Since the

pass/fail results correspond to cells, then it would have been obvious to make the address of the cell with pass or fail result be addressable by an X (x-axis direction) and Y (y-axis direction) pin.

As per claim 19,

Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads.

Double Patenting (non-statutory)

4. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); In re Vogel, 422 F.2d 438,164 USPQ 619 (CCPA 1970); In re Van Omum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) and In re Goodman, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 3 7 CFR 1. 3 2 1 (b) and may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4.1 **Claim(s) 6** of patent # **6,564,346** contain(s) every element of **claim(s) 1** of the instant application and as such anticipates **claim(s) 1** of the instant application.

4.1.1 "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over

claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

4.2.1 This is a provisional obviousness-type double patenting.

Claim Rejections - 35 USC ' 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5.1 Claims 1,3-10 and 12-19 are rejected under 35 U.S.C. 102 (e) as being anticipated by Vollrath et al. (US Patent No. 6,564,346; filed: December 7, 1999).

Vollrath et al. discloses all the limitations of Claims 1,3-10 and 12-19 in Figs. 1-10 and related description in col. 1 line 3- col. 12 line 33.

The applied reference has a common inventor **Vollrath** with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
10/1/04